



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,472	12/30/2003	Michael L. Combs	BUR920000163US2	7077
30449	7590	10/28/2004	EXAMINER	
SCHMEISER, OLSEN + WATTS SUITE 201 3 LEAR JET LATHAM, NY 12033			TSAI, CAROL S W	
			ART UNIT	PAPER NUMBER
			2857	

DATE MAILED: 10/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,472	COMBS ET AL.	
	Examiner	Art Unit	
	Carol S Tsai	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 21 September 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 3-11 and 20-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 8-11 and 20-26 is/are allowed.
- 6) Claim(s) 3-7,27 and 28 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3, 4, 7, 27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,397,361 to Saitoh.

With respect to claims 3 and 4, Saitoh discloses a method of testing a semiconductor chip having a plurality of common I/Os associated therewith, the method comprising the steps of: connectivity testing a chip-to-package connection of at least one of the common I/O of the plurality of common I/Os, wherein the connectivity testing comprise: launching a transition through the common I/O to an associated I/O package connection and pad; and observing a response of the transition (see col. 3, lines 37-54 and col. 11, line 51 to col. 13, line 17); determining whether the chip-to-package connection is faulty from a result of the connectivity testing (see col. 8, line 62 to col. 10, line 25 and col. 13, lines 17-21); and triggering a first latch at an initialization of the transition response and triggering a second latch when the transition response has reached a transition threshold value (see col. 7, lines 9-60 and col. 9, line 7 to col. 10, line 25).

As to claim 7, Saitoh also discloses the driver being configured as a weak driver that is sensitive to capacitative loading (see col. 10, lines 14-25).

As to claims 27 and 28, Saitoh also disclose providing semiconductor circuitry between the driver and the control I/O (switch latch circuit 203 and 204 and receiver 1202 shown on Fig. 13).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent No. 6,397,361 to Saitoh in view of U. S. Patent No. 6,262,580 to Wu.

With respect to claims 5 and 6, Saitoh discloses a method of testing a semiconductor chip having a plurality of common I/Os associated therewith whose characteristics or properties can be tested by applying a test signal through a control I/O, the method comprising the steps of: connectivity testing a chip-to-package connection of at least one of the common I/O (see col. 3, lines 37-54 and col. 11, line 51 to col. 13, line 17); and determining whether the chip-to-package connection is faulty from a result of the connectivity testing (see col. 8, line 62 to col. 10, line 25 and col. 13, lines 17-21).

Saitoh does not disclose determining whether the chip-to- package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity

testing of a first I/O with a second RC constant associated with a second signal relating to a connectivity testing of a second I/O.

Wu teaches determining whether the chip-to- package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity testing of a first I/O with a second RC constant associated with a second signal relating to a connectivity testing of a second I/O (see col. 2, lines 9-24 and col. 3, line 26 to col. 4, line 65).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Saitoh's method to include determining whether the chip-to-package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity testing of a first I/O with a second RC constant associated with a second signal relating to a connectivity testing of a second I/O, as taught by Wu, in order to test whether the integrated circuit can function properly.

Allowable Subject Matter

6. Claims 8-11 and 20-26 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

U. S. Patent No. 6,397,361 to Saitoh is the reference closest to the claimed invention. Saitoh discloses a method of testing a semiconductor chip having a plurality of common I/Os associated therewith, the method comprising the steps of: connectivity testing a chip-to-package connection of at least one of the common I/O of the plurality of common I/Os, wherein said connectivity testing comprises generating a transition signal from a driver of the common I/O, and wherein the driver is configured as a weak driver that is sensitive to capacitive loading;

determining whether the chip-to-package connection is faulty from a result of the connectivity testing. However, Saitoh does not teach placing additional impedance into connection with the driver prior to generating the transition signal; and including all of the other limitations in the respective independent claims.

Response to Arguments

7. Applicant's arguments filed September 21, 2004 have been fully considered but they are not persuasive.

Applicants argue that Saitoh does not disclose and triggering a first latch at an initialization of the transition response and triggering a second latch when the transition response has reached a transition threshold value. The Examiner disagrees with applicants. Since it is well known in the art a latch is a circuit or circuit element used to maintain a particular state, such as on or off, open or close, or logical true or false in which a latch changes state only in response to a particular input; therefore, as set forth above in the art rejection, Saitoh does disclose triggering a first latch at an initialization of the transition response and triggering a second latch when the transition response has reached a transition threshold value (see col. 7, lines 9-60 and col. 9, line 7 to col. 10, line 25; Specifically, tester 205 inputs switch latch data corresponding to a particular switch (e.g., 608) associated with a true I/O (e.g., 620) to change the state of the switch from an open state to a closed state. With switch 608 in a closed state, FM True I/O 206 is now in circuit communication with true I/O 620 through switch bus 302 and closed switch 608. Since all other switches (e.g., 604, 610, and 612) are in the open state, true I/O 620 is the only chip I/O in circuit communication with tester 205. With such a configuration, after all of the chip I/O

drivers are tri-stated (i.e., completely open), tester 205 forces a small current into true I/O 620 and measures the voltage associated with the forced current. Consequently, if the measured voltage associated with the forced current is zero, very nearly zero, or below a predetermined threshold voltage, such measured voltage is indicative of a short-circuit to ground in the true I/O 620).

Applicants argue that claim 5 is not unpatentable over Saitoh in view of Wu, because Saitoh in view of Wu does not teach or suggest each and every feature of claims. For example, Saitoh does not teach or suggest the feature: “determining whether the chip-to- package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity testing of a first I/O with a second RC constant associated with a second signal relating to a connectivity testing of a second I/O”. The Examiner disagrees with Applicants. As set forth above in the art rejection, Saitoh discloses the claimed invention except for determining whether the chip-to- package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity testing of a first I/O with a second RC constant associated with a second signal relating to a connectivity testing of a second I/O. Wu teaches determining whether the chip-to- package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity testing of a first I/O with a second RC constant associated with a second signal relating to a connectivity testing of a second I/O (see col. 2, lines 9-24 and col. 3, line 26 to col. 4, line 65), in order to test whether the integrated circuit can function properly. Therefore, the combination of Saitoh and Wu clearly teach the claimed invention.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for TC 2800 is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (571) 272-1585 or (571) 272-2800.

Art Unit: 2857

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.



Carol S. W. Tsai

Patent Examiner

Art Unit 2857

10/19/04